Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN

[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]

Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 7026

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – JUNE / JULY 2024

Second Semester

VLSI Design

P23VD206 – TESTING AND VERIFICATION OF VLSI CIRCUITS

(Regulation 2023)

Time: Three Hours

Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	State any 2 differences between IEEE 1149.1 and IEEE 1500 standard.	2	K1	CO1
2.	Relate the scope of testing and verification in VLSI design.	2	K1	CO1
3.	Consider a chip with 100,000 gates and 2,000 flip-flops. A combinational ATPG program produced 500 vectors to fully test the logic. What is the number of clock cycles required for testing using a single scan-chain design and find gate overhead?	2	K1	CO2
4.	Show that the three single faults, H s-a-1, J s-a-1, and K s-a-1, are equivalent.	2	K1	CO2
5.	Interpret non-robust path delay test and a robust path delay test.	2	K2	CO3
6.	List the various types of idempotent faults.	2	K1	CO3
7.	Recall the importance of true value simulation techniques.	2	K1	CO4
8.	Name any four methods in test generation for combinational circuits.	2	K1	CO4
9.	Relate formal and functional verification.	2	K1	CO5
10.	Compare model checking and equivalence checking.	2	K1	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.	Questions	Marks	KL	CO
11. a)	A Manufacturer of an IC performs two types of tests on its product: *defect testing* and *speed binning*.			
	i. The type 1 test is for *defect testing* to sort out defective devices from the good devices. Based on its fabrication and experience, the manufacturer has found that 96% fault coverage is sufficient for the IC manufactured by it. The area of the IC is 0.60 sq. cm., the fault density is 1.5 faults/sq. cm., and the fault clustering factor is 0.15. Infer the defect level in the devices that pass type 1 test performed for defect testing.	4	K1	CO1
	ii. The type 2 test is performed only on the ICs which pass the type 1 test, i.e. are expected to be defect free. Type 2 test is for speed binning. The objective here is to divide all the ICs into two bins, fast bin and slow bin. Devices which are in the fast bin can run at 1.5 GHz or more (faster ICs) and are sold at higher price relative to the devices which are in slow bin (slower ICs). The following information is given about this testing stage. Of all the devices that passed defect test it is known that 30% of them are truly fast and 70% of them are truly slow. However, the speed binning test is not perfect and the Figure 1 gives different probabilities for a device to be in the fast or slow bin. a. Among devices that are tested by type 2 test, find the percentage of those will appear in the fast bin. b. Find the max percentage of devices that are sold as fast ICs, are likely to be returned as either slow devices or defective devices. You can assume that type 2 test is unable to perform defect testing and defective devices that pass the type 1 test are uniformly distributed.	9		

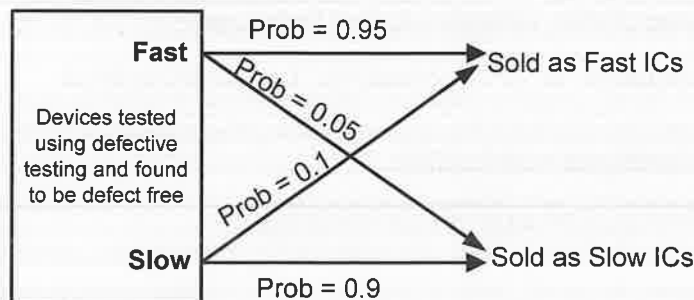


Figure 1

(OR)

b) Product details and process parameters of an IC being designed and fabricated by a manufacturer are as follow: | 13 | K1 | CO1

Area of the IC = 0.75 sq cm.

Fault density = 1.45 faults/sq cm

Clustering factor = 0.11

Cost of producing a chip = $ 0.75 (This is the cost of producing each chip before it is tested)

A chip that is tested good will be sold for $ 4.00

Cost of replacing a bad chip = $ 15.00

The manufacturer of the IC use test T1 provides fault coverage of 90%. The manufacturer wishes to produce 1 million chips for selling i.e. after testing the manufacturer would like to have 1 million devices that are tested "good".

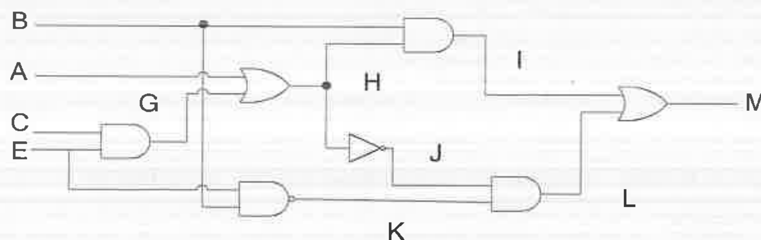
i. Find the defect level for the devices tested by the test T1 express it in ppm (parts per million).

ii. For the test T1 find the cost of producing 1 million chips that well be sold, i.e. chips that are tested "good".

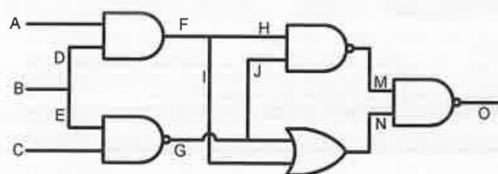
iii. For the chips tested by the test T1 determine the total cost of replacing the bad chips.

iv. What will be the total profit for the chips tested by T1?

12. a) i. Consider the two bridge faults in the following circuits: OR-type bridge fault between C and E, and OR-type bridge fault between J and K. Find all test patterns which can distinguish these two faults. | 8 | K1 | CO2

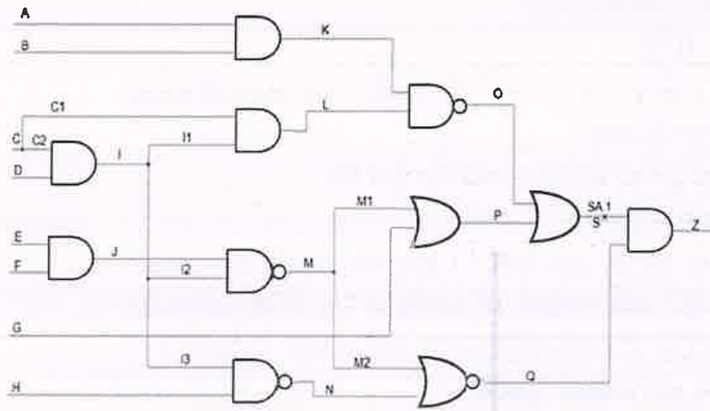


ii. Perform deductive fault simulation for the test vector A=1, B=0, C=1 for the circuit shown in figure below. | 5



(OR)

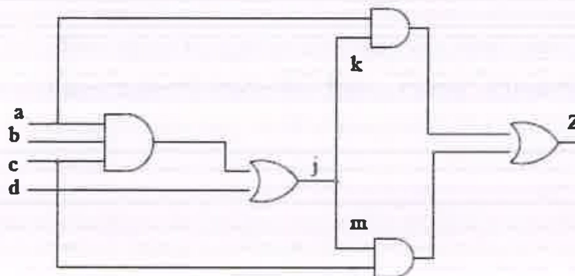
b) i. Construct the FAN algorithm to derive a test for the fault S stuck-at-1 in the circuit shown in figure below. SCOAP testability measures are shown. Neatly write all steps, objectives, operations (backtrace, forward implications etc.). 10 K3 CO2



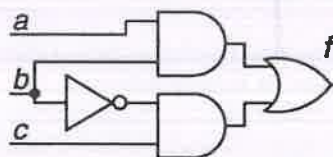
ii. For the circuit shown below, using the method of Boolean differences, construct a set of all tests that detect single stuck-at faults 3

a. j *s-a-1*

b. k *s-a-0.*



13. a) For the circuit given below, assume an exhaustive binary up counter based pattern generator. K3 CO3



i. Construct an internal XOR single input signature response analyzer (SISR) with characteristic equation $1+x^2+x^3$. 4

ii. Apply the good machine signature for the circuit. Assume SISR is initialized to "000" before testing. 3

iii. Apply the bad machine signature for the faults given below and check if these faults will be detected by the SISR 6

a. b stuck-at-1.

b. f stuck-at-1

(OR)

b) i. Relate whether each of the polynomials given below is primitive. Give proof for your answers. — 9 — K2 — CO3

a. $1 + x + x^4$
b. $1 + x + x^2 + x^3 + x^4$
c. $1 + x^3 + x^4$

Sketch the standard and modular XOR realization of the above polynomials

ii. Consider the following RAM test algorithm. — 4

$\Uparrow(W0) \Uparrow (R0,W1,R1) \Uparrow (R1,W0,R0)$

Given below are different two-coupling faults. Find the faults that are detected by the above test algorithm assuming that RAM contains 1M cells. Also explain when will the fault be excited and when will it be detected.

a. A change in the contents of cell 600 causes cell 10005 to change
b. A change in the cell content 30018 causes cell 0 to change

14. a) i. Apply event-driven simulation technique for the circuit given in Fig. 1a. Delay of two-input gates - 1 ns, Delay of three-input gates -1.2 ns; Delay of inverter - 0.6 ns. Assume the inputs are changing as shown in Fig. 1b. Show all events and activity lists of each time stamp. Also draw the final waveform — 10 — K2 — CO4

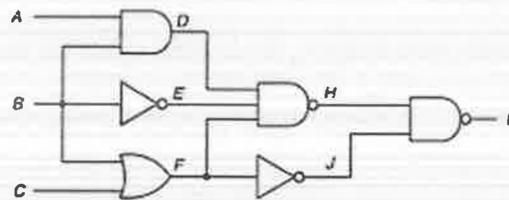


Fig. 1a

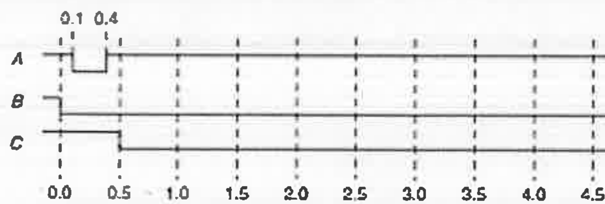


Fig. 1b

ii. What are the advantages of using formal methods for design verification. — 3

(OR)

b) Explain with examples — 5 — K2 — CO4

i. Computational Tree Logic — 5

ii. Kripke structure — 3

iii. Boolean satisfiability problem

15. a) Consider the circuits in Fig. 1a and Fig. 1b — 13 — K3 — CO5

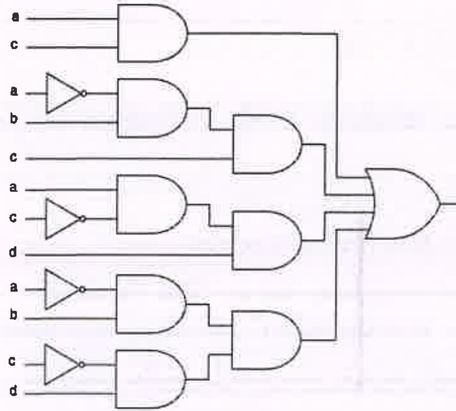


Fig. 1a

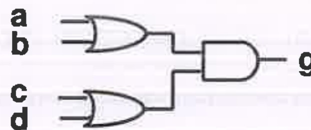


Fig. 1b

Identify the functional equivalence of the logic circuit in Fig.1a with that of Fig. 1b using ROBDDs. Prove your answer.

(OR)

b) Consider the figure shown below and assume the timing parameters, setup time, $t_s = 0.6$ ns, hold time $t_h = 0.4$ ns, and clock to Q delay is in the range $0.8 \leq t_{cq} \leq 1$ ns, the propagation delay through AND and XOR gate is 1.2ns and propagation delay through NOT gate is 1.1ns. The delays introduced in the clock paths are represented as Δ_1, Δ_2, and Δ_3. — 13 — K3 — CO5

a. Identify the maximum clock frequency without any violations when

   i. $\Delta_1 = \Delta_2 = \Delta_3 = 0$

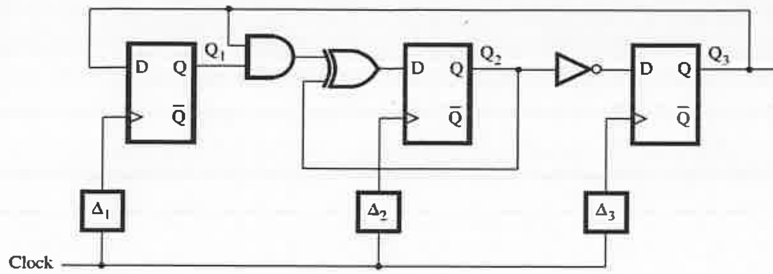
   ii. $\Delta_1 = 1$ns, $\Delta_2 = 0$, $\Delta_3 = 0.5$ns

b. Identify the paths with and without hold time violations when

   i. $\Delta_1 = \Delta_2 = \Delta_3 = 0$

   ii. $\Delta_1 = 1$ns, $\Delta_2 = 0$, $\Delta_3 = 0.5$ns

Show calculations for all the paths in each case. Provide proper justification for the answers



PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16. a)		In the Boundary scan standard Explain the TAP controller with state diagram also mention the state through which tap controller goes in of these instructions.	15	K2	CO2
		(OR)			
b)	i.	Find the SCOAP testability measures of each line in the circuit below.	7	K4	CO2
	ii.	Apply PODEM algorithm to generate a test for the line 13 s-a-0 in the following circuit. Show the steps in the form of the table given below.	8